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M. Coli and S. Lupini: A NEW BILATERAL FAST LINEAR GATE CIRCUIT. -

(Nota interna: n. 242)

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A NEW BILATERAL FAST LINEAR GATE CIRCUIT. -

SUMMARY. -

A linear gate for 1 ns minimum width pulse is described. The minimum gate duration is 5 ns, the rejection ratio for non-gated pulses is 30 db at maximum amplitude of 120 mA output pulse. Attenuation of allowed pulses is 0. 7 db. A gating pulse generator is also described capable of repetition rates up to 100 Mc/sec.

CHARACTERISTICS. -

Gated pulses circuit. -

Input pulses:	
Polarity	positive and negative
Amplitude	0 - 120 mA
Impedance	50 Ohm
Maximum pulse width	$\sim$ 3 ns (less than formed gating pulse width)
Minimum pulse width	$\sim$ 1 ns
Output pulses:	
Polarity	positive and negative
Impedance	$\cong$ 50 Ohm
Attenuation (with gating pulse)	$\cong$ 0. 7 db
Attenuation (without gating pulse)	= 30 db (at maximum amplitude)
Fed through/fed back through signal ratio	> 20)
A. c. pedestal (pic to pic)	< 8 mA
D. c. pedestal	< 2 mA

Gating pulse shaper. -

Input pulses:	
Trigger polarity	negative
Amplitude	4 - 40 mA
Impedance	50 Ohm
Maximum pulse width	less than the delay of the forming cable
Minimum pulse width	1 ns
Output pulses:	
Polarity	negative
Amplitude	18 mA
Width	10, 20 ns
(variable with cable length	from 5 ns minimum
Rise and fall time (10-90%)	3 ns (measured on 330 Ohm)
Cable characteristics:	RG174/21-598 50 Ohm (5,2 ns/m delay)

INTRODUCTION. -

The gate herein presented (fig. 1) can be used linearly with pulses of 1 ns width up to 120 mA amplitude, with minimum gating width of 5 ns, at repetition rate of 100 Megapulses/sec.

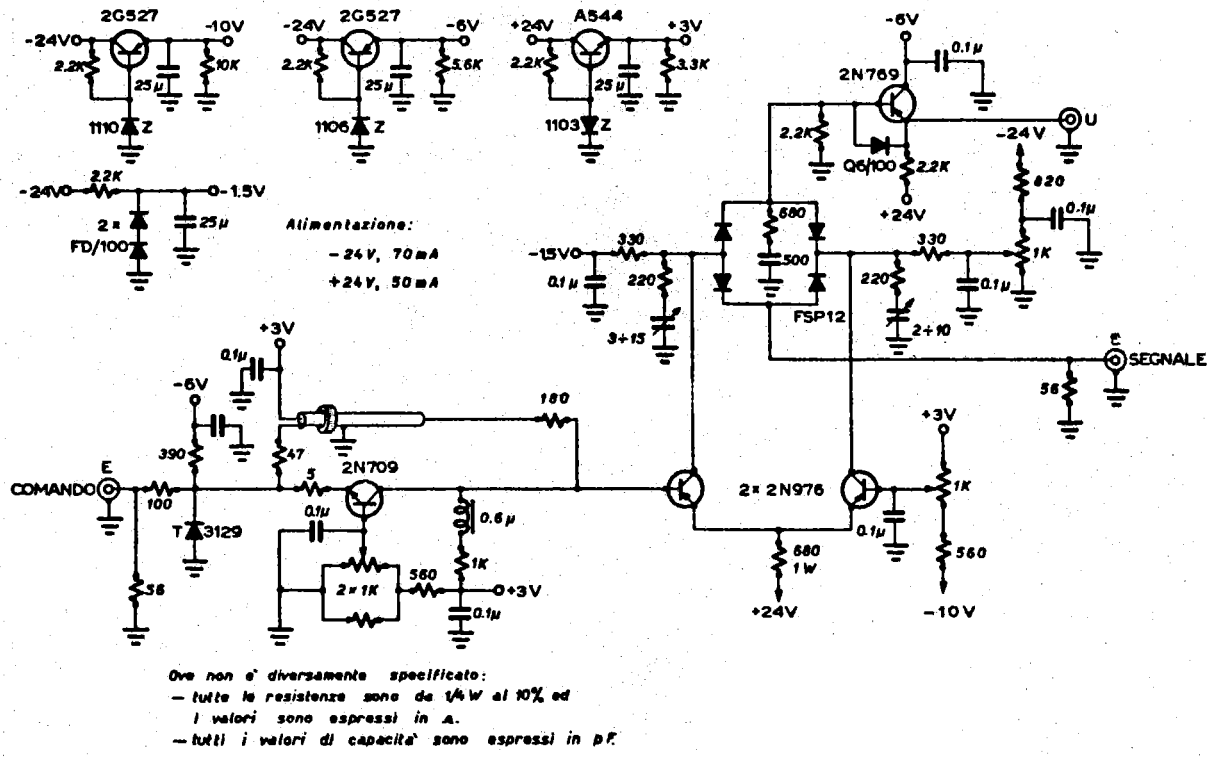


FIG. 1

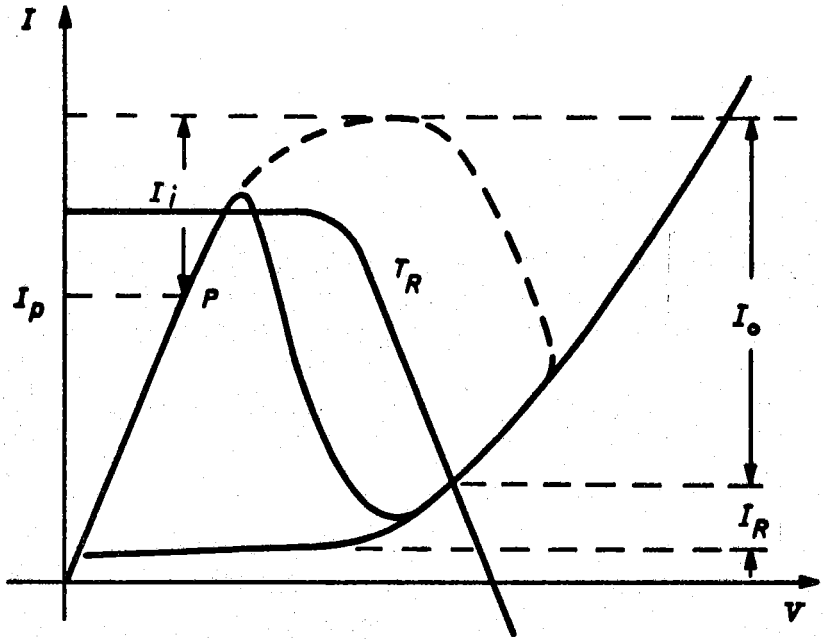
The circuit herein presented utilizes some nanosecond current steering technique applied to a balanced diode bridge, to be open to transmit pulses through the output linearily. Current steering is performed by a balanced common emitter pair of fast transistors[1]. The diode bridge is realized on the same silicon wafer with planar techniques. They are now commercially available with diode controlled characteristic within 10%[2].

During the last few years many efforts have been done about sampling balanced diode bridge. The problem to be solved here is exactly the inverse being gating pulses wider than allowed ones. Diode bridge technique has given us the opportunity to utilize for a fast linear gate the pulse bilaterality with the very good inherent linearity of the up to date commercially available diode compounds.

The hybrid tunnel diode common base transistor coupling technique has ben used[3] in a gating pulse shaper, with profit. The circuit has few components and allows minimum gating pulse width in the nanosecond range. Repetition rate of formed pulses is over 100 MHz.

GATING PULSE SHAPER. -

The circuit is formed by a 1N3129 tunnel diode dynamically loaded with the input impedance of a common base transistor in such a way to remain in a bistable condition.



I_p biasing current

I_i amplitude of input current pulse

I_R amplitude of current reset pulse

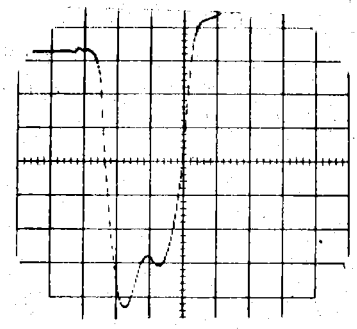
I_0 amplitude of current pulse delivered to the output load transistor

FIG. 2

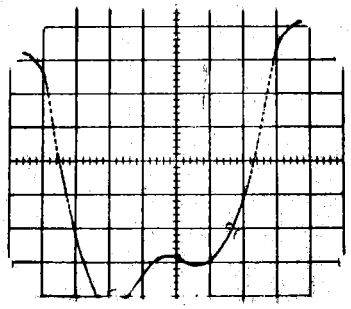
A common-base transistor acts as an unilateral buffer at the output of the diode.

The diode is statically biased in its low-voltage region with 16 mA. The input pulse brings the diode into its high-voltage region; a current of about 15 mA is fed into the load transistor and remains in this region till the reset pulse comes in through the cable[4]. Fig. 2 shows the switching path in the V-I plane of the diode.

A part of the current transferred through the transistor is inverted by a cable transformer and fed back after the cable delay to reset the diode. With two meters of RG 174/U cable the pulses is 12 ns wide (fig. 3); transistor time transfer is about 0. 8 ns; deadtime is less than 10 ns(5).



5 ns x cm
0. 5 V x cm



2 ns x cm
0. 5 V x cm

FIG. 3 - Output current pulse of the gating pulse shaper (on 180 Ohm load).

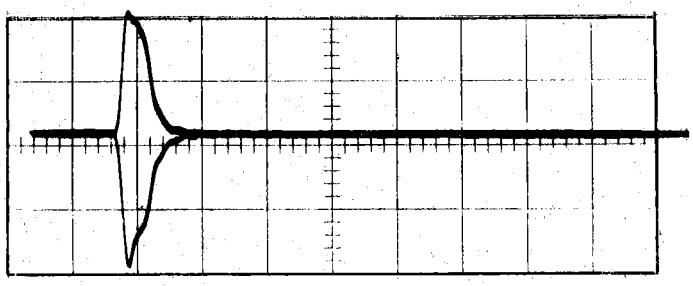


FIG. 4

Gating pulses at the long tail pair output.

CURRENT SWITCHING WITH THE LONG-TAIL PAIR. -

The circuit is formed by two 2N976 transistors mounted in a balanced common emitter pair. The circuit, as known, has very good current switching properties. In fact currents can change between transistors contemporarily and in the same amount. The total switching time ($\sim$2 ns) is firstly determined by the cut-off frequency of transistors common collector connection.

The first transistor is off and receives the switching signal from the output of the gating pulse shaper.

The output on the collectors are two pulses of opposite polarities, and equal amplitude ($\sim$4V). The delay depends only on the switchingtime delay difference between the two transistors (fig. 4). We have measured a maximum delay of 0. 8 ns.

GATE CIRCUIT. -

A fast silicon junction four diode bridge diffused on the same slide form the circuit (fig. 5).

The pulses from the long-tail-pair activate the branches ACB-ADB of the bridge, statically biased on the reverse region with 1.5 V. The pulses to be fed through the bridge are applied to point D and picked up from point C. This is a simple way to gate pulses of opposite polarities in a perfect bilateral manner. In the two opposite branches of the bridge will flow the same gating pulse current, if the static characteristics of the diode are identical.

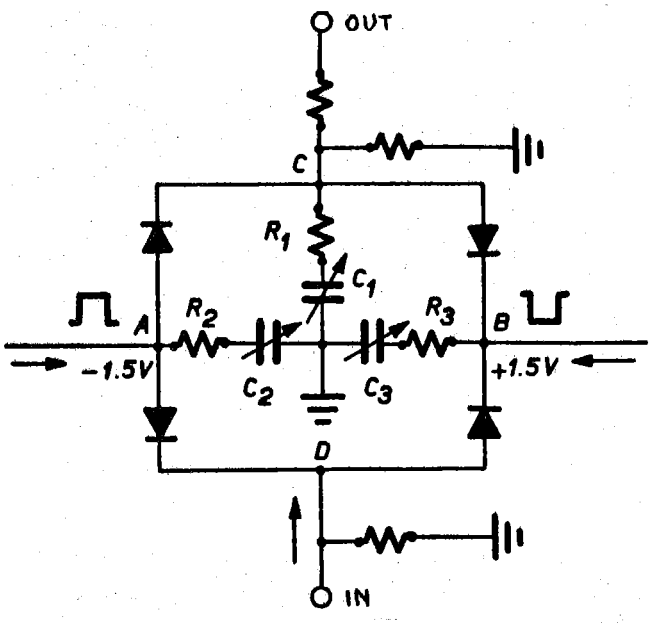


FIG. 5

No d. c. pedestal will be present in the output and if the reactive components of the branches are also identical, no a. c. pedestal will also be present (see fig. 6 for d. c. considerations).

Some amplitude difference of the gating pulses originates d. c. pedestal in the output; difference in shape or different delays give rise to a. c. pedestals.

The reactive components in the branches which give rise to the output pedestals are mainly due to the reverse region capacitance of the diodes. 1.5 V reverse bias on the diodes assure little capacitance and low voltage excursions in the current switching circuit, at the same time.

With a reference to the pulses to be fed through the bridge, we must also consider the dynamic reactance of the diodes. Difference between bran

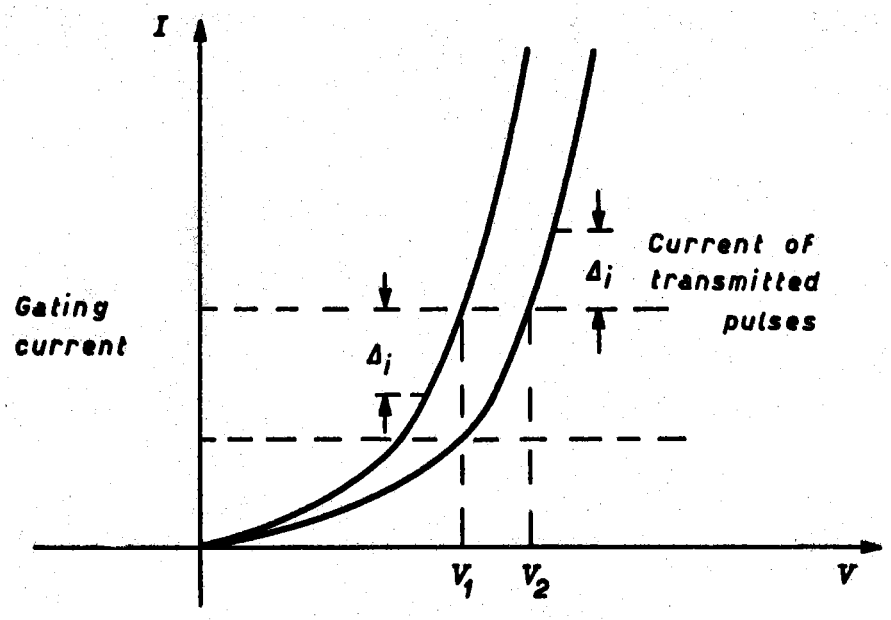
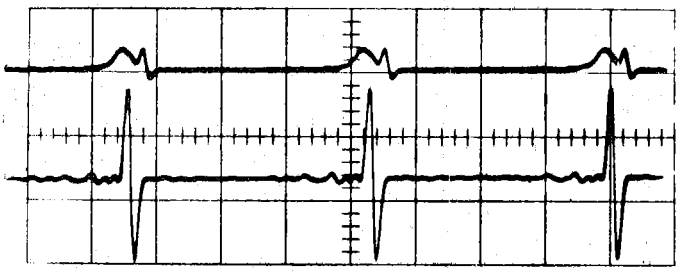


FIG. 6

ches produces attenuation dependent on shape and width of the allowed pulses and maximum transfer current limitation. It is possible to compensate for little ohmic and reactive differences in the branches with RC parallel networks (fig. 5). The compensation can be effective only in a limited range of frequencies, that means, only for some gating and gated pulse widths. Experimentally we could find very good adjustments. We have obtained 200 mV a. c. and 40 mV d. c. pedestal, feed through/feed back through signal ratio better than 25 (a. c.) (240 mV with maximum dynamics) (fig. 7 and fig. 9).



1. 50 ns 0. 1V / cm
2. 50 ns 0. 2V / cm

FIG. 7

2 V / cm
50 ns / cm

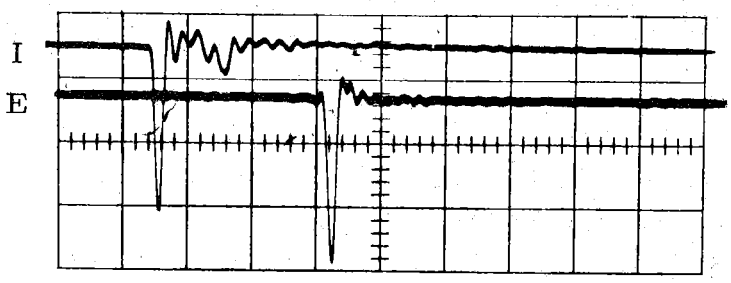
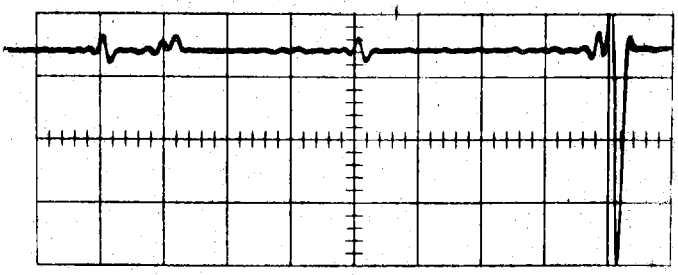


FIG. 8



1 V / cm
50 ns / cm

FIG. 9

The attenuation for gated pulses is less than 0. 7 db (fig. 8).

It is fairly easy to lower the pedestal with the above shown technique. Further improvements can be achieved at a cost of more attenuation.

The linearity is shown in fig. 10.

MATCHING OF THE GATED PULSES. -

A perfect matching of input and output pulses of the bridge can be realized only with two buffer circuits.

Good matching can be provided, avoiding circuit complexity, for gated and non gated pulses, with an output emitter-follower. This can provide a 10 KOhm input impedance so that the input impedance of allowed pulses can be separated quite completely from the output. Large dynamics are assured with little currents from gating pulses in the diodes.

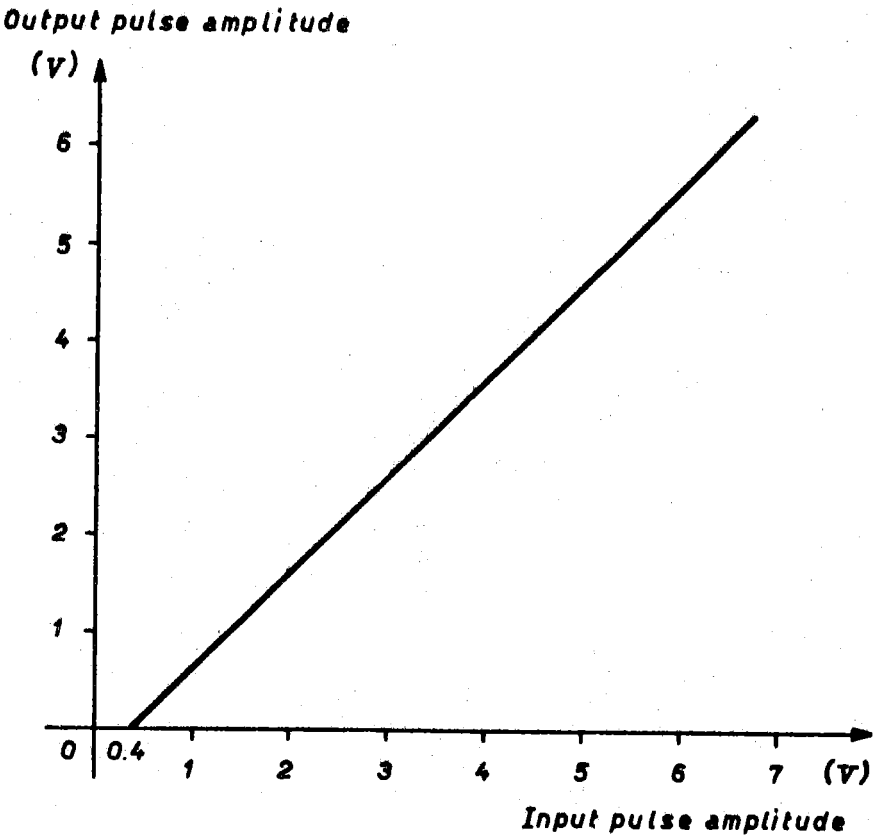


FIG. 10 - Linearity curve between input and output pulses.

ACKNOWLEDGEMENTS. -

Authors wish to thank Mr. C. Dardini for useful discussions and suggestions regarding the balanced bridge diode use.

REFERENCES. -

(1) - A. Barna and J. H. Marshall, Inst. of Techn., Pasadena (1959).
(2) - see Fairchild FSP12 or other products under request.
(3) - Amadei P. J. and Kosanocky W. F., R. C. A. Rev. 22, 669 (1961).
(4) - For the principle see Sugarman monostable circuit.
(5) - M. Coli and A. Serra, "Two circuit modules of an automatic pulse selection and registration unit", Presented at SFER Nuclear Electronic, Paris, 1963; Laboratori Nazionali di Frascati, LNF-64/17 (1964).